UNITED STATES PATENT AND TRADEMARK OFFICE

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LSI LOGIC CORPORATION
1621 BARBER LANE
MS D-106, LEGAL DEPARTMENT
MILPITAS, CA 95035

EXAMINER
PARK, ILWOO

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 30

Application Number: 09/183,694
Filing Date: October 30, 1998
Appellant(s): ELLIS ET AL.

Christopher P. Mariorana

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/29/2002.

(1)   Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2)   Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly

affect or be directly affected by or have a bearing on the decision in the pending appeal

is contained in the brief.

(3)   *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4)   *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection

contained in the brief is correct.

(5)   *Summary of Invention*

The summary of invention contained in the brief is deficient because it only

supports for a portion of claims.

Re-ordering may be found in page 3, lines 23-26, page 4, lines 1-3, page 8, lines

20-22, page 40, lines 27-28, page 41, lines 5-7, page 43, lines 15-17, page 44, lines 15-

17, page 45, lines 1-3, and page 46, lines 18-19.

Generating interrupts at beginning and at end of the plurality of commands would

be found in page 3, lines 17-22

(6)   *Issues*

The appellant's statement of the issues in the brief is correct.

(7)   Grouping of Claims

The examiner respectfully disagree with the reasons in the appellant's response

filed on 2/4/2003 containing claims do not stand or fall together because merely pointing

out differences in what the claims cover is not an argument as to why the claims are

separately patentable: i.e., the appellant's arguments do not provide the reasons why

the claims are separately patentable between each of groups I and II, groups I and III,

groups I and IV, groups I and V, groups II and III, groups II and IV, groups II and V,

groups III and IV, groups III and V, and groups IV and V.

(8)   Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9)   Prior Art of Record

5,781,803	KRAKIRIAN	7-1998
5,483,641	JONES et al	1-1996
4,543,626	BEAN et al	9-1985

(10)   Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim 21, 22, and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by

Krakirian, US patent No. 5,781,803.

As to claim 21, Krakirian teaches a data controller [hard disk controller IC 204] of

a peripheral device [target device 202 in figs. 3 and 4; col. 7, lines 7-24] having a

storage medium [hard disk 208] and a processor [microprocessor 206], wherein the

data controller data controller minimizes interrupts [elimination of an interrupt to the

microprocessor for seeking operation in case that reordered commands parsed by the

controller are contiguous disk block accesses each other: col. 3, lines 38-42; col. 16,

line 34-col. 17, line 5; col. 17, lines 36-63] to the processor by re-ordering [col. 15, lines

13-28] a plurality of commands received from a host computer [initiator 201] from an

order of arrival into an order of sequence in the storage medium.

As to claim 22, Krakirian teaches a command queuing engine configured to

arrange the plurality of commands into at least one thread [col. 17, lines 40-51].

As to claim 26, Krakirian teaches a peripheral device [target device 202 in figs. 3

and 4; col. 7, lines 7-24] that includes a data controller [hard disk controller IC 204],

microprocessor [206], a buffer memory [205], local memory and a storage medium [hard

disk 208], and that is couplable to a host [initiator 201], wherein the data controller

creates [col. 17, lines 40-63] threads of a plurality of commands and generates

interrupts [col. 4, lines 4-43] at the beginning and end of the of the plurality of

commands relative to a data transfer.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krakirian,

US patent No. 5,781,803 and Jones et al., US patent No. 5,483,641.

As to claim 3, Krakirian teaches a data controller [hard disk controller IC 204 in

figs. 3 and 4], that is couplable to a host [initiator 201] and coupled to a storage

medium, microprocessor, local storage and a buffer memory, comprising a command

queuing engine that creates a plurality of threads of sequential commands [col. 15, lines

18-27; col. 17, lines 36-63] while minimizing [col. 5, lines 8-12] interrupts associated to

the commands. Even though Krakirian teaches creating a plurality of threads of

sequential commands, Krakirian does not explicitly disclose the plurality of threads of

sequential commands exist simultaneously.

Jones et al teach a data controller queues a plurality of commands, reorders the

commands, and creates a plurality of threads of sequential commands [multiple

sequential read or write requests; a plurality of COMB-ORIGs] that exist simultaneously

[col. 6, lines 10-21; col. 50, lines 50-60; col. 53, lines 1-63].

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to combine the teachings of Krakirian and Jones et al

because they both teach holding a plurality of commands in a command queue,

reordering the commands for sequential accesses, and creating threads for accesses of

a hard disk drive and the Jones et al's teaching of the plurality of threads of sequential

commands existing simultaneously in a queue would increase efficiency of seek

operation by reordering of a plurality of commands and making threads as many as

possible for the commands in the queue of Krakirian.

Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Krakirian, US patent No. 5,781,803 and Jones et al., US patent No. 5,483,641 as

applied to claim 3 above, and further in view of Bean et al., US patent No. 4,543,626.

As to claims 16 and 18, Bean et al teach a command queuing engine comprises:

a transfer extend generator configured to generate [col. 4, lines 38-42] transfer

extend entries for a data transfer between the storage medium and a host computer;

and

a data retrieval channel [col. 6, lines 64-68] coupled to receive the transfer

extend entries for programming the data transfer.

As to claim 19, Bean et al teach the command queuing engine further comprising

a status retrieval channel [col. 3, lines 59-64; col. 4, lines 18-21].

As to claim 20, Bean et al teach each of the retrieval channels are coupled to

receive transfer extend entries and to provide [implicit: col. 7, lines 29-57] used read

pointers to a first storage device of the peripheral device.

As to claim 17, Bean et al teach the transfer extend generator is coupled to the

buffer memory to store the transfer extend entries [col. 4, lines 15-18].

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to combine the teachings of Krakirian, Jones et al, and

Bean et al because they both teach a data controller [Bean et al: e.g., host interface

controller processor 12 and source processor 18 in fig. 1] for receiving commands from

a host and a microprocessor [Bean et al: e.g., disk controller processor 14 in fig. 1] for

performing hard disk access operations in accordance with the host commands

received and queued and the Bean et al's teaching of generating transfer extend entries

from the host commands would increase efficiency by further reducing interrupts [col.

12, lines 32-43 of Krakirian and col. 2, lines 3-17 and col. 6, lines 23-32 of Bean et al] to

the microprocessor of Krakirian and Jones et al.

Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Krakirian, US patent No. 5,781,803 as applied to claim 21 above, and further in view of

Bean et al., US patent No. 4,543,626.

As to claims 23-25, Bean et al teach the limitations of the claimed invention [vide

supra].

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to combine the teachings of Krakirian and Bean et al

because they both teach a data controller [Bean et al: e.g., host interface controller

processor 12 and source processor 18 in fig. 1] for receiving commands from a host and

a processor [Bean et al: e.g., disk controller processor 14 in fig. 1] for performing hard

disk access operations in accordance with the host commands received and queued

and the Bean et al's teaching of generating transfer extend entries from the host

commands would increase efficiency by further reducing interrupts [col. 12, lines 32-43

of Krakirian and col. 2, lines 3-17 and col. 6, lines 23-32 of Bean et al] to the processor

of Krakirian.

(11)   Response to Argument

The Examiner summarizes the various points raised by the Appellants and addresses replies individually.

The Appellants argue in substance that a) Krakirian does not show that a data controller reorders a plurality of commands while suspecting the reordering of Krakirian could be done by a processor [microprocessor 206] not by a data controller [hard disk controller 204], b) Krakirian discloses not minimizing interrupts rather shows that the microprocessor 206 is interrupted upon receipt of each command [col. 12, lines 35-40], c) Krakirian does not disclose or suggest a data controller creating a plurality of threads of a plurality of commands, and d) no motivation to modify Krakirian with Jones et al,

For the point a), firstly, the claim 21 does not clearly describes which element (either a data controller, a processor, or other element) re-orders the commands, secondly, as seen the support in *(5) Summary of Invention* above, if the re-ordering is provided by a processor (firmware) not a data controller, then Krakirian's re-ordering perfectly fits, and lastly, if, while no support being found, the re-ordering is provided not by a processor but by a data controller, then: Krakirian teaches a burst of commands each having a disk block address to access are received into a command queue [col. 15, lines 13-33] and parsed [col. 17, lines 45-47] by the hard disk controller 204, then the hard disk controller 204 interrupts [col. 12, lines 32-43] the microprocessor 206 for the seek operation. The parsing includes analyzing a block address for seeking and accessing a storage medium of a hard disk. The examiner respectfully disagree that the microprocessor 206 performs the reordering commands in sequential order because

Krakirian never disclose the microprocessor doing reordering, it would be a duplication of analyzing a block address, and it would be an another interrupt to the microprocessor contrary to Krakirian's intention of reducing interrupts.

For the point b), not meaning that the microprocessor must be interrupted upon receipt of each command, Krakirian teaches interrupts are maskable [col. 12, lines 44-67] and further teaches if access operation of the storage medium is for accessing sequential block addresses, then the access operation is treated as a single command operation (one of a thread) even though the access operation is analyzed from a plurality of commands [col. 17, lines 36-63]; consequently, the seek operation for each command of the plurality of commands is not needed and the microprocessor is not required to be interrupted for the each command.

For the point c), though Krakirian only discloses an example of creation of a single thread of a plurality of commands as explained above, inherently another creation of a thread of a plurality of commands would happen again and again or from time to time for accessing sequential block addresses of a storage medium of a hard disk [it's hardly imaginable that another creation of a thread never happen since the creation of the single thread in a lifetime of hard disk operation].
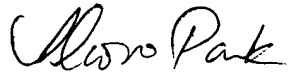
And for the point d), Krakirian teaches holding a plurality of commands in a command queue, reordering the commands for sequential accesses, and creating a thread for sequential accesses. And Jones et al teach holding a plurality of commands in a command queue, reordering the commands for sequential accesses, and creating threads that exists simultaneously in the queue. Therefore, one of ordinary skill in the

art would be easily motivated from the Jones et al's teaching of the more threads for

more efficiency in disk accessing.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Ilwoo Park
April 17, 2003

Conferees

Christopher B. Shin

Jeffrey A. Gaffin

LSI LOGIC CORPORATION
1551 McCarthy Blvd., MS: D-106
Patent Law Department
Milpitas, CA 95035